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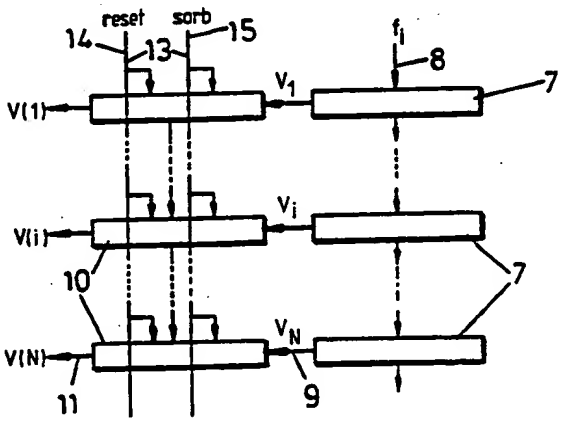
(54) Title: SOLID STATE IMAGING DEVICE



(57) Abstract

The present invention relates to solid state imaging or devices and in particular to such devices provided with electronic exposure control means. The device comprises a 2-D array of sensing cells (3), and horizontal and vertical scanning means (4, 5) coupled to each cell (3). The vertical scanning means (5) comprises a plurality of vertical scanning lines (11), each commonly connected to sensing cells (3) arranged in a horizontal direction (12), and vertical shift register means (6) having outputs connected to the vertical scanning lines (11) for driving them with control pulses so as to cause each line to be successively reset and then sampled after a variable period defining an integration time. The vertical shift register means comprises a single vertical shift register (6) formed and arranged to be driven with an input *fi* so as to drive a group of successive vertical scanning lines (11) during each line period. Global reset and sample signal drive means are connected (14, 15) to each of said lines (11) via a decode cell (10), each of which is connected to the decode cells (10) of preceding and succeeding lines $i + 1$ and $i - 1$. The decode cells (10) are formed and arranged so that the leading line i of the group of lines from $i + n + 1$ to N and 1 to i being reset is sampled, the number of lines in the group being reset determining the number of lines in a group ahead of the sampled line i which are not being reset and hence the integration time, whereby the integration time may be varied by variation of the input *fi* to the vertical shift register (6). The present invention also provides a method of automatically electronically controlling exposure using a solid state image pick-up device of the invention.

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SOLID STATE IMAGING DEVICE

The present invention relates to solid state imaging or image pick-up devices and in particular to such devices provided with electronic exposure control means.

It is known that exposure control in apparatus incorporating solid state image pick-up devices can be realised electronically - rather than mechanically using iris means - by varying the integration time of the sensor cells i.e. the period of time after resetting of the sensor cells during which they are exposed to light before they are sampled. The arrangements previously used for varying the integration time have though been relatively complex and cumbersome including, for example, the use of multiple vertical shift registers.

It is an object of the present invention to avoid or minimise one or more of the above disadvantages.

The present invention provides a solid state image pick-up device comprising a two-dimensional array of sensing cells, each sensing cell having a photodiode and a transistor for reading from and writing to the photodiode, horizontal and vertical scanning means coupled to each cell of the array, wherein said vertical scanning means comprises a plurality of vertical scanning lines, each commonly connected to sensing cells arranged in a horizontal direction, and vertical shift register means having outputs connected to the vertical scanning lines for driving the vertical scanning lines with control pulses so as to cause each line to be successively reset and then sampled after a variable period defining an integration time, characterised in that the vertical shift register means comprises a single vertical shift register formed and arranged to be driven with an input so as to drive a group of

successive vertical scanning lines during each line period, and there are provided global reset and sample signal driven means connected to each of said lines via a decode cell, each said decode cell being connected to the decode cells of preceding and succeeding lines, said decode cells being formed and arranged so that the leading line of the group of lines being reset is sampled, the number of lines in the group being reset determining the number of lines in a group ahead of the sampled line which are not being reset and hence the integration time, whereby the integration time may be varied by variation of the input to the vertical shift register.

With a solid state image pick-up device of the present invention it is possible to control exposure electronically in a simple and economic manner with only one vertical shift register thereby minimising the overall size and hence area of circuitry required on the integrated circuit semi-conductor chip and hence facilitating maximal miniaturisation of the device.

It will be appreciated that various combinations of logic gates may be used to realise the decode cell, including arrangements with as few as four logic gates as will be further described hereinbelow.

Further preferred features and advantages of the present invention will appear from the following detailed description given by way of example of a preferred embodiment illustrated with reference to the accompanying drawings in which:

Fig. 1 is a general schematic plan view of a solid state image pick-up device of the type disclosed in our earlier International Patent Publication No. WO 91/04633;

Fig. 2 is a detail view showing part of the vertical

shift register of the device of Fig. 1 with associated decode cells and connections thereto;

Fig. 3 is a schematic representation of the status of the various lines in the device of Figs. 1 and 2 at any given time;

Fig. 4 is a detail view showing the internal architecture of an individual decode cell;

Figs. 5 to 7 showing waveforms for the vertical shift register input, the reset signal, and a comparison of the waveforms for different lines at any given time; and

Fig. 8 illustrates a suitable control algorithm for exposure control.

Fig. 1 shows a solid state image pick-up device 1 comprising a two-dimensional array 2 of sensing cells 3 coupled to horizontal and vertical scanning means 4 and 5, respectively. The vertical scanning means comprises a vertical shift register 6 containing a plurality of vertical shift register cells 7 having a common input line 8 for receiving input signals f_i and each connected 9 via a respective decode cell 10 to a vertical scanning line 11 connected in turn to a horizontal row 12 of sensing cells 3 (see Fig. 1). Each of the decode cells 10 is also commonly connected 13 to global reset and sampling lines 14 and 15, respectively.

The vertical shift register input signal f_i is made up of a block of reset control pulses for enabling resetting of a number of the vertical scanning lines 11 - lines i+n+1 to N and 1 to i leaving lines i+1 to i+n "integrating" i.e. "recording" the light falling on them until they are sampled - see Fig. 3. As shown in Fig. 5 the number of pulses in the block may be varied so that at any given moment any number from just one to all of the lines are reset - corresponding to maximum number of lines "integrating" and hence maximum integration period

resulting in maximum exposure and vice versa respectively. As shown in Figs. 2 and 4, all the lines 11 receive a reset signal via the global reset line 14. Only those lines 11 receiving control reset signals via the respective vertical shift register cells 7 are however actually reset.

As may be seen from Fig. 7, the sample signal received via the global sampling line 15, is timed ahead of the reset signal received via the global reset line 14 so that the sampled line i is sampled prior to being reset. The decode cell 10 is formed and arranged so that whilst all the lines 11 receive a sample signal via the global sampling line 15, only line i, the first line in the block of lines being reset is actually sampled.

Fig. 4 shows one particular way of realizing the above arrangement. In more detail the decode cell comprises a NOR gate 16 and three NAND gates 17, 18, 19. The NOR gate 16 monitors the presence of a reset control signal from the respective vertical shift register cell 7 and provides an output X, to the first NAND gate 17 of the decode cell 10 of the next vertical scanning line i+1 and to a second NAND gate of the decode cell of line i. Thus the first NAND gate 17 of each decode cell 10 compares the "reset" status of the present line i and the previous line i-1, the leading edge of the block of "reset" lines corresponding to the absence of "reset" status on the present line (at the time of sampling - see below) and presence of "reset" status on the previous line. The third NAND gate 19 then uses the output of the second NAND gate 18 to enable sampling only at that line i at the leading edge of the block of "reset" lines. In this way sampling and then resetting of a variable number of lines (corresponding to variable exposure times) can be controlled simply by means of

providing blocks of reset control pulses of variable size through the vertical shift register. It will of course be appreciated that Fig. 4 represents only one way of achieving the desired control of sampling using global sampling and reset inputs and control pulse inputs via the (single) vertical shift register and that various other forms of decode cell may also be used.

By means of the above arrangement a relatively wide range of different exposure values may be achieved depending on the total number of vertical scanning lines used. An even greater degree of exposure control allowing particularly short exposure times may be achieved by varying the length of the actual reset signal as shown in Fig. 6. It will be appreciated that by shortening the reset signal (but still maintaining the same starting time) in line i+1 where this is the next line to be sampled (i.e. the block of reset control pulses covers the maximum number of lines) then the length of the relatively short integration period available before sampling, can be varied thereby providing an additional dimension in exposure variation.

The actual values which should be used to set the exposure times (via the number of lines to be reset and/or the length of the reset pulses) may be readily determined by any suitable means including for example measurement of grey level histograms of previous images and/or measuring the percentages of pixels with values above or below two or more grey scale thresholds, and then comparing these against predetermined criteria. One example of a suitable system is illustrated with reference to Fig. 8 which is an automatic exposure control decision diagram. In this case the video stream is internally histogrammed by pixel brightness into three bins: very white, average, and very black. Where

the image is found to be nearly all black it is judged to be too dark and the exposure increased. Conversely when the image is found to be nearly all white it is judged to be too bright and the exposure reduced.

In a further aspect the present invention provides a method of automatically electronically controlling exposure in a solid state image pick-up device comprising a two-dimensional array of sensing cells, each sensing cell having a photodiode and a transistor for reading from and writing to the photodiode, horizontal and vertical scanning means coupled to each cell of the array, wherein said vertical scanning means comprises a plurality of vertical scanning lines, each commonly connected to sensing cells arranged in a horizontal direction, and vertical shift register means having outputs connected to the vertical scanning lines for driving the vertical scanning lines with control pulses so as to cause each line to be successively reset and then sampled after a variable period defining an integration time, which method comprises the steps of providing an input to the vertical shift register so as to drive a group of successive vertical scanning lines with control signals for enabling resetting thereof during each line period, providing global sampling and reset signals to all the vertical scanning lines, and processing the signals received at each line so as to enable sampling of a vertical scanning line at the leading edge of said group of successive vertical scanning lines, monitoring the image obtained with said pick-up device and varying said input to the vertical shift register so as to increase or decrease the number of lines in said group of successive vertical scanning lines thereby to decrease or increase the integration period of the vertical scanning lines, respectively.

As used herein the "line period" is the period required to sample a line and progress to the next line to be sampled.

It will be noted from Fig. 7 that the global sample signal is transmitted ahead of the global reset signal so that when the present line "reset status" input to the first NAND gate 17 is 'read' to determine enabling or non-enabling of sampling, the "reset status " for the present line will be effectively that from the previous line period.

CLAIMS

1. A solid state image pick-up device comprising a two-dimensional array of sensing cells, each sensing cell having a photodiode and a transistor for reading from and writing to the photodiode, horizontal and vertical scanning means coupled to each cell of the array, wherein said vertical scanning means comprises a plurality of vertical scanning lines, each commonly connected to sensing cells arranged in a horizontal direction, and vertical shift register means having outputs connected to the vertical scanning lines for driving the vertical scanning lines with control pulses so as to cause each line to be successively reset and then sampled after a variable period defining an integration time, characterised in that the vertical shift register means comprises a single vertical shift register formed and arranged to be driven with an input so as to drive a group of successive vertical scanning lines during each line period, and there are provided global reset and sample signal driven means connected to each of said lines via a decode cell, each said decode cell being connected to the decode cells of preceding and succeeding lines, said decode cells being formed and arranged so that the leading line of the group of lines being reset is sampled, the number of lines in the group being reset determining the number of lines in a group ahead of the sampled line which are not being reset and hence the integration time, whereby the integration time may be varied by variation of the input to the vertical shift register.

2. A device as claimed in claim 1 wherein the decode cells comprise a NOR gate and three NAND gates, said NOR gate being formed and arranged for monitoring the presence of a reset control signal from the respective

vertical shift register cell and providing an output to a first said NAND gate of the decode cell of the next vertical scanning line i + 1, and to a second NAND gate of the decode cell of line i, said second NAND gate being also coupled to a global reset input, and providing an output to a third NAND gate also coupled to the output of the first NAND gate to enable sampling only at that line i at the leading edge of the block of lines being reset.

3. A device as claimed in claim 1 or claim 2 wherein is provided a reset signal control means formed and arranged for varying the duration of the reset signal.

4. A device as claimed in any one of claims 1 to 3 wherein is provided an automatic exposure control means comprising histogramming means formed and arranged for histogramming the video stream output of the device into a plurality of different pixel brightness levels, comparator means formed and arranged for comparing the histogram obtained with stored histogram data, and reset signal control means formed and arranged for increasing or decreasing the number of lines being reset in response to excursions of said histogram outside predetermined histogram profiles defined by said stored histogram data, so as to restore the video stream pixel brightness profile within said predetermined histogram profiles whereby exposure is automatically controlled so as to avoid excessively dark or excessively bright images.

5. A method of automatically electronically controlling exposure in a solid state image pick-up device comprising a two-dimensional array of sensing cells, each sensing cell having a photodiode and a transistor for reading from and writing to the photodiode,

horizontal and vertical scanning means coupled to each cell of the array, wherein said vertical scanning means comprises a plurality of vertical scanning lines, each commonly connected to sensing cells arranged in a horizontal direction, and vertical shift register means having outputs connected to the vertical scanning lines for driving the vertical scanning lines with control pulses so as to cause each line to be successively reset and then sampled after a variable period defining an integration time, which method comprises the steps of providing an input to the vertical shift register so as to drive a group of successive vertical scanning lines with control signals for enabling resetting thereof during each line period, providing global sampling and reset signals to all the vertical scanning lines, and processing the signals received at each line so as to enable sampling of a vertical scanning line at the leading edge of said group of successive vertical scanning lines, monitoring the image obtained with said pick-up device and varying said input to the vertical shift register so as to increase or decrease the number of lines in said group of successive vertical scanning lines thereby to decrease or increase the integration period of the vertical scanning lines, respectively.

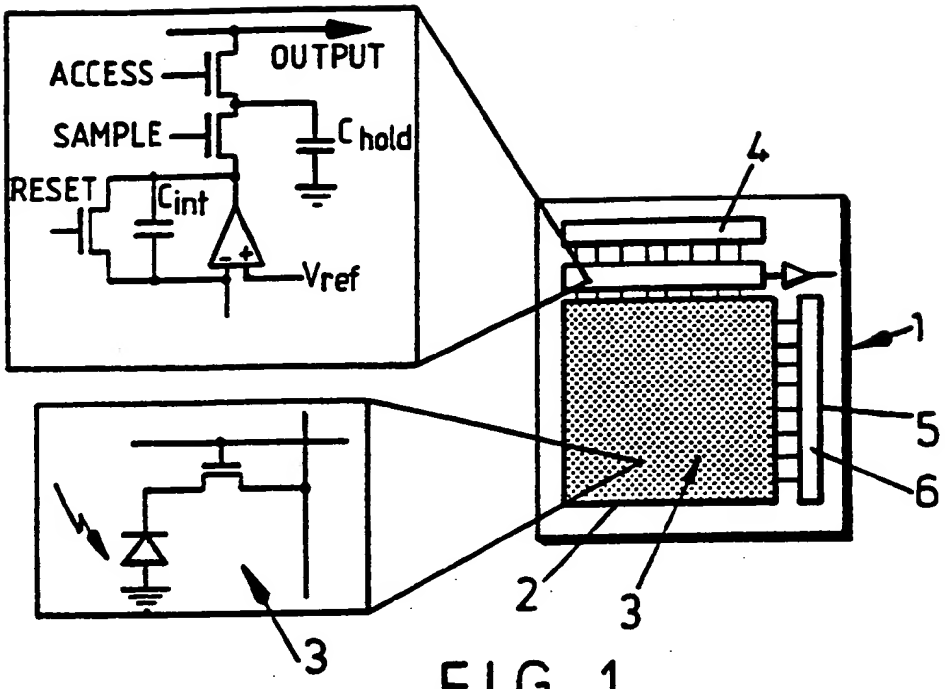
ACCESS
OUTPUT
SAMPLE
C hold
RESET
Cint
Vref
4
1
5
6
2
3
3

FIG. 1

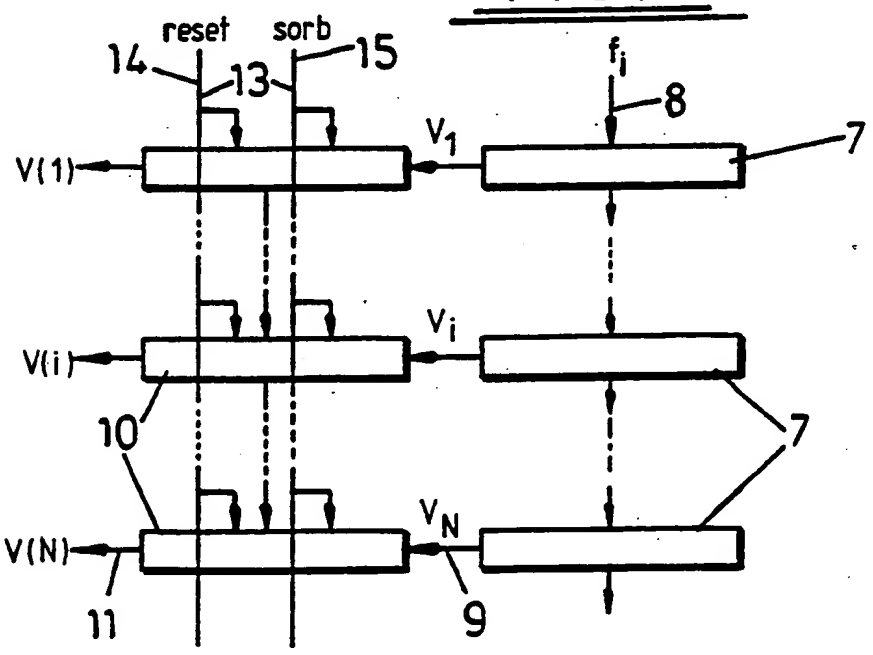
reset
sorb
14
13
15
fi
8
V1
7
V(1)
Vi
V(i)
10
7
VN
V(N)
11
9

FIG. 2

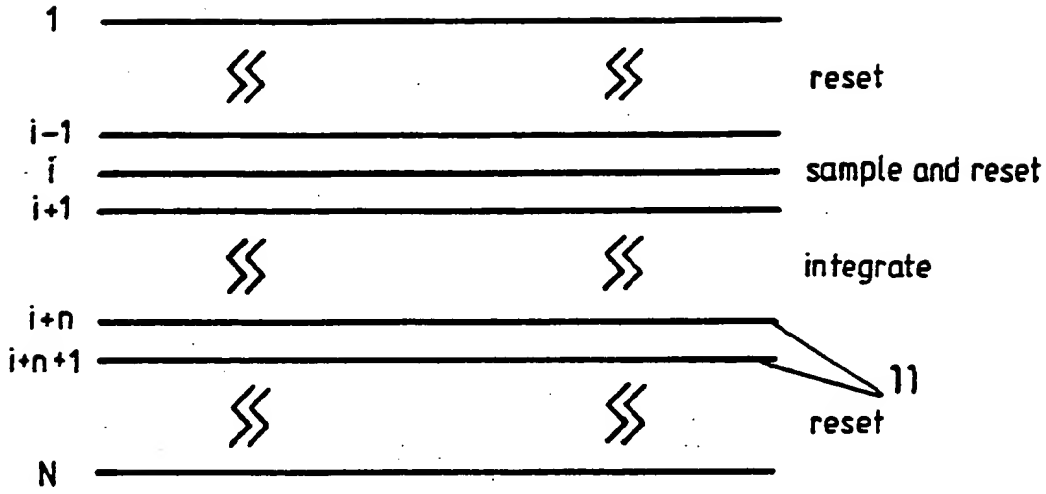
1
reset
i-1
i
sample and reset
i+1
integrate
i+n
i+n+1
11
reset
N

FIG. 3

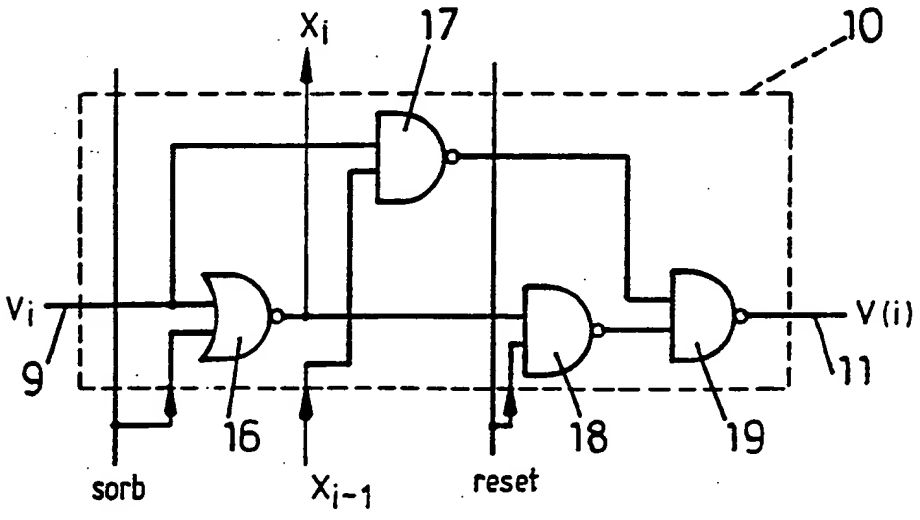
Xi
17
10
Vi
9
16
sorb
Xi-1
reset
18
19
V(i)
11

FIG. 4

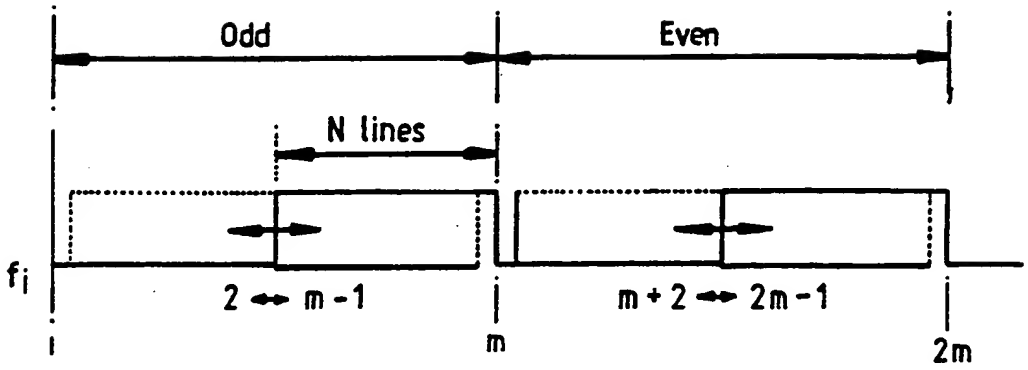
Odd
Even
N lines
f_i
2 ↔ m - 1
m + 2 ↔ 2m - 1
m
2m

FIG. 5

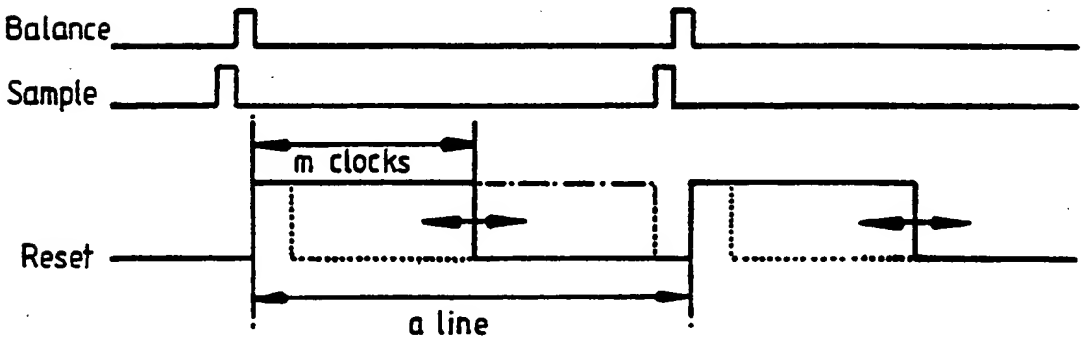
Balance
Sample
m clocks
Reset
a line

FIG. 6

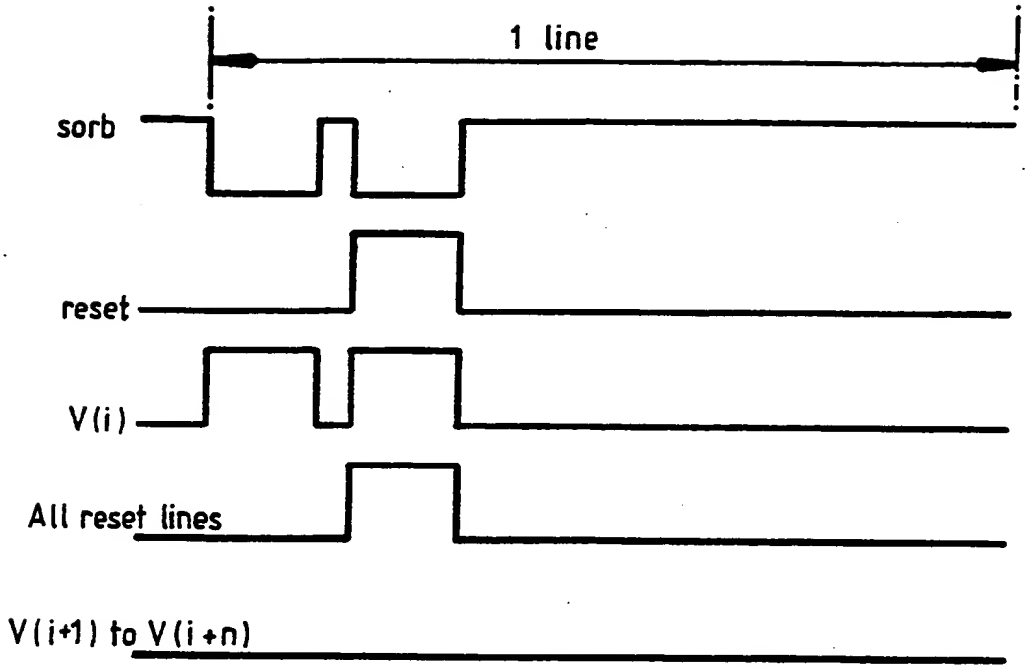
1 line
sorb
reset
V(i)
All reset lines
V(i+1) to V(i+n)

FIG. 7

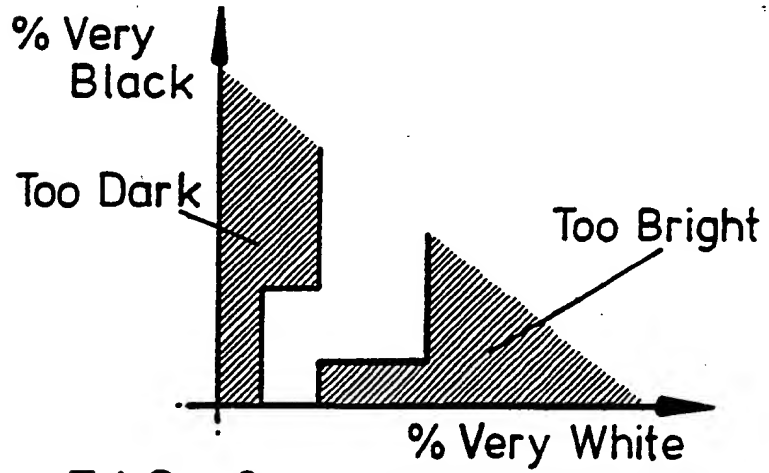
% Very Black
Too Dark
Too Bright
% Very White

FIG. 8

INTERNATIONAL SEARCH REPORT

PCT/GB 92/01522

International Application No

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all)[6]

According to International Patent Classification (IPC) or to both National Classification and IPC

Int.Cl. 5 H04N3/15

II. FIELDS SEARCHED

Minimum Documentation Searched[7]

Classification System	Classification Symbols
Int.Cl. 5	H04N

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched[8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT[9]

Category °	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No.[13]
A	PROCEEDINGS OF THE IEEE 1990 CUSTOM INTEGRATED CIRCUITS CONFERENCE 16 May 1990, BOSTON US pages 731 - 734 RENSHAW.D 'asic vision' see the whole document	1,5
A	US,A,5 027 217 (OSHIO ET AL.) 25 June 1991 see column 6, line 33 - column 8, line 45; figures 2,3	1,5
A	FR,A,2 538 652 (THOMSON CSF) 29 June 1984 see page 3, line 26 - page 5, line 8; figure 1	1,5

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IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
29 OCTOBER 1992	09. 11. 92
International Searching Authority	**Signature of Authorized Officer**
EUROPEAN PATENT OFFICE	BEQUET T.P.

Form PCT/ISA/210 (second sheet) (January 1985)

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON INTERNATIONAL PATENT APPLICATION NO. GB 9201522 SA 63630

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US-A-5027217	25-06-91	JP-A- 1231485	14-09-89
FR-A-2538652	29-06-84	None	